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SCHEIBEL, ROBERT C	
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2419	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/826,668	WYBENGA ET AL.	
	Examiner	Art Unit	
	ROBERT C. SCHEIBEL	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-16 and 19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 10-16, and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Examiner acknowledges receipt of Applicant's Request for Continued Examination (RCE) filed 8/17/2009.
- Claims 1, 10, and 19 are currently amended.
- Claims 1-7, 10-16, and 19-23 are currently pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/14/2009 and RCE filed on 8/17/2009 have been entered.

Response to Arguments

2. Applicant's arguments, see pages 10-13, filed 7/14/2009, with respect to the rejection of claims 1-8, 10-16, and 19-23 under 35 U.S.C. 103(a) have been fully considered but they are not persuasive.

On page 10, Applicant summarizes the current amendment as well as the rejections mailed in the Final Office Action on 5/14/2009. On page 11, Applicant summarizes independent claim 1. On page 12, Applicant describes the rejection of claim 1 under 35 U.S.C. 103(a) and asserts that the combination of Calvignac, Fallon , and Cheriton does not disclose the limitation

that one of said first and second security and classification functions is performed according to information from the routing table search circuit. Applicant further argues that independent claims 10 and 19 contain analogous limitations and that claims 2-7, 11-16, and 20-23 depend from one of these claims and are thus allowable for similar reasons.

Examiner respectfully disagrees. As described in the previous rejection, Cheriton discloses the limitations of the routing table search circuit in at least Figure 2A which is a block diagram of a packet classifier. Since the function of a classifier clearly includes at least classification functions, Cheriton also discloses the limitation that "one of said first and second security and classification functions is performed according to information from the routing table search circuit" because at least some information from the routing table search circuit is used to ultimately determine the packet classification. Therefore, the above combination of Calvignac, Fallon, and Cheriton does make the limitations of claim 1 (as well as claims 10 and 19) obvious under 35 U.S.C. 103(a).

Claim Objections

3. Claims **1 and 10** are objected to because of the following informalities:

- In line 5 of claim 1, "routing nodes:" should be corrected to "routing nodes comprises:".
- In line 6 of claim 10, "routing nodes:" should be corrected to "routing nodes comprises:".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims **1, 6, 7, 10, 15, 16, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2003/0231625 to Calvignac et al in view of U.S. Patent 7,415,540 to Fallon et al and in further view of U.S. Patent Application 2006/0104286 to Cheriton.

Regarding claims **1 and 10**, Calvignac discloses a router for interconnecting external devices coupled to said router, said router comprising:

a switch fabric (switch fabric 60 of Figure 2 and the switch fabric not shown in Figure 4A which connects to the switch interfaces (see paragraph 37 on page 4)); and

a plurality of routing nodes coupled to said switch fabric (router blades 80, 90, and 100 of Figure 2; note that element 150 of Figure 4A is also a router blade), wherein each of said plurality of routing nodes comprises:

a first network processor (the ingress portion of the router blade shown in Figure 4B; this can be implemented as a single chip/processor as indicated in the last sentence of paragraph 3 on page 1) for performing first security and classification functions (see the description of the classification and security (firewall) functions throughout; consider paragraphs 5 on page 1 and 47 on page 5) associated with data packets received from said external devices and transmitted to said switch fabric (the ingress circuitry of Figure 4B; this circuitry clearly processes packets received from the external devices and transmitted to the switch fabric); and

a second network processor (the egress portion of the router blade (analogous to the ingress portion shown in Figure 4B); this can be implemented as a single chip/processor as indicated in the last sentence of paragraph 3 on page 1) for performing second security and classification functions (see the description of the classification and security (firewall) functions throughout; consider paragraphs 5 on page 1 and 47 on page 5) associated with data packets received from said switch fabric and transmitted to said external devices (the egress circuitry analogous to the ingress circuitry of Figure 4B; this circuitry clearly processes packets received from the switch fabric and transmitted to the external devices).

Further regarding claim **10**, Calvignac discloses the communication network in Figure 1.

Similarly regarding claim **19**, Calvignac discloses the method limitations which are analogous to the claim 1 limitations as above.

Calvignac does not disclose expressly the limitation that the first network processor comprises a first plurality of microengines; the limitation that the first plurality of microengines performs the first security and classification functions; or the limitation that each data packet is distributed to a selected microengine. Calvignac also does not disclose the limitation that the second network processor comprises a second plurality of microengines; the limitation that the second plurality of microengines performs the second security and classification functions; or the limitation that each data packet is distributed to a selected microengine.

However, Fallon discloses a router (10 in Figure 1) implemented using a multithreaded microprocessor (12 in Figure 1) which includes multiple microengines (22 in Figure 1). Fallon discloses that the received datagrams/packets are assigned (by the scheduler thread 318) to a particular processing thread (320a, 320b, etc. of Figure 3; see lines 16-21 of column 6, for example). Further, as indicated in lines 11-13 of column 2, for example, each microengine runs a particular thread. Thus, the packets are distributed to a selected microengine via the scheduler thread 318.

Calvignac and Fallon are analogous art because they are from the same field of endeavor of packet communications routing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Calvignac to implement each of the ingress and egress processors to using the microengine implementation of Fallon. This combination of Calvignac and Fallon discloses the missing limitations of claims 1, 10, and 19 that the first and second network processors comprise a plurality of microengines (each of the first and second network processors will comprise multiple microengines 22 as in Fallon); that the first and second plurality of microengines perform the security and classification functions (in the

combination of Calvignac and Fallon, the security and classification functions performed by the ingress and egress processors will be implemented by the microengines); and that each data packet is distributed to a selected microengine (in the above combination of Calvignac and Fallon, when a packet is assigned to a thread, it is distributed to a particular microengine.)

The motivation for doing so would have been to improve processing efficiency by providing a multithreaded implementation and doing so by minimizing the amount of time required to maintain packet order and data coherency as suggested in lines 17-25 of column 1.

However, the combination of Calvignac and Fallon does not disclose expressly the limitation of claims 1, 10, and 19 that each of the routing nodes comprises a routing table search circuit comprising an initial content addressable memory stage followed by a plurality of trie tree search table stages, wherein one of said first and second security and classification functions is performed according to information from the routing table search circuit. However, Cheriton discloses the limitation of a routing table search circuit comprising an initial content addressable memory stage followed by a plurality of trie tree search table stages (see Figure 2A which shows a packet classifier comprised of an initial content addressable memory stage (203) followed by a plurality of trie tree search table stages (204 – which includes one or more trie tables in one embodiment; see further, paragraph 0021 on page 3 which clearly indicates that this packet classifier is used to assist in routing table lookup (by making it more efficient than the prior art solution with a separate entry in the TCAM for each host)). Further, since Figure 2A describes a block diagram of a packet classifier and the function of a classifier clearly includes at least classification functions, Cheriton also discloses the limitation that "one of said first and second security and classification functions is performed according to information from the routing table

search circuit" because at least some information from the routing table search circuit is used to ultimately determine the packet classification.

Calvignac and Cheriton are analogous art because they are from the same field of endeavor of packet switching systems. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Calvignac, as modified above, to add a routing table search circuit with an initial CAM stage followed by a plurality of trie tree search table stages similar to that disclosed in Cheriton. The motivation for doing so would have been to improve the efficiency of the routing function as suggested by Cheriton in paragraph 0021. Therefore, it would have been obvious to combine Cheriton with Calvignac and Fallon for the benefit of improved efficiency to obtain the invention as specified in claims 1, 10, and 19.

Regarding claims **6 and 15**, the above combination of Calvignac, Fallon and Cheriton discloses the limitations of parent claims 1 and 10. Calvignac does not expressly disclose the limitations of claims 6 and 15 that a first one of said first plurality of microengines is capable of executing N threads, wherein each of said N threads performs at least one security and classification function.

However, Fallon discloses the limitations of claims 6 and 15 that a first one of said first plurality of microengines is capable of executing N threads, wherein each of said N threads performs at least one security and classification function (see lines 11-13 of column 2 which indicates that each microengine is capable of running N threads (N=4 in that particular example); see also lines 37-65 of column 5 and lines 16-21 of column 6 which indicate that the processing threads are used to process the datagram/packet; as indicated above, in the combination of

Calvignac and Fallon, the classification and security functions of Calvignac are processed by these threads, so each thread performs at least one security and classification function).

Calvignac and Fallon are analogous art because they are from the same field of endeavor of packet communications routing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Calvignac to implement each of the ingress and egress processors to using the microengine implementation of Fallon where each microengine can support multiple threads.

The motivation for doing so would have been to improve processing efficiency by providing a multithreaded implementation and doing so by minimizing the amount of time required to maintain packet order and data coherency as suggested in lines 17-25 of column 1. Therefore, it would have been obvious to combine Fallon and Cheriton with Calvignac for the benefit of improved processing efficiency to obtain the invention as specified in claims 6 and 15.

Regarding claims **7 and 16**, the above combination of Calvignac, Fallon and Cheriton discloses the limitations of parent claims 6 and 15. Calvignac does not expressly disclose the limitations of claims 7 and 16 that a first one of said second plurality of microengines is capable of executing M threads, wherein each of said M threads performs at least one security and classification function.

However, Fallon discloses the limitations of claims 7 and 16 that a first one of said second plurality of microengines is capable of executing M threads, wherein each of said M threads performs at least one security and classification function (see lines 11-13 of column 2 which indicates that each microengine is capable of running M threads (M=4 in that particular

example); see also lines 37-65 of column 5 and lines 16-21 of column 6 which indicate that the processing threads are used to process the datagram/packet; as indicated above, in the combination of Calvignac and Fallon, the classification and security functions of Calvignac are processed by these threads, so each thread performs at least one security and classification function).

Calvignac and Fallon are analogous art because they are from the same field of endeavor of packet communications routing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Calvignac to implement each of the ingress and egress processors to using the microengine implementation of Fallon where each microengine can support multiple threads.

The motivation for doing so would have been to improve processing efficiency by providing a multithreaded implementation and doing so by minimizing the amount of time required to maintain packet order and data coherency as suggested in lines 17-25 of column 1. Therefore, it would have been obvious to combine Fallon and Cheriton with Calvignac for the benefit of improved processing efficiency to obtain the invention as specified in claims 7 and 16.

7. Claims **2, 5, 11, 14, 20, and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 20030231625 to Calvignac et al in view of U.S. Patent 7,415,540 to Fallon et al in view of U.S. Patent Application 2006/0104286 to Cheriton and in further view of U.S. Patent 7,197,035 to Asano.

The above combination of Calvignac, Fallon and Cheriton discloses the limitations of parent claims 1, 10, and 19. However, combination of Calvignac, Fallon and Cheriton does not disclose expressly the limitations of dependent claims 2, 5, 11, 14, 20, and 23.

Regarding claims 5, 14, and 23, Asano discloses said security and classification functions comprise performing a Network Address Translation (NAT) function to provide subnet independence throughout. Consider, for example, lines 34-41 of column 3 which describes an efficient NAT function as an object of Asano's inventions. Further, the Asano discloses the limitations of claims 2, 11, and 20 that the security and classification functions comprise replacing a source address associated with header information of a first data packet with an address selected from a pool of router addresses associated with said router in lines 27-35 of column 11 as well as lines 20-33 of column 12. These passages explain that the local source addresses of computers 12-x are replaced by a global address of the router and that this global address is selected from a pool of IP addresses. Calvignac and Asano are analogous art because they are from the same field of endeavor of high-speed packet processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to explicitly add well known network address translation (NAT) functionality to the combination of Calvignac, Fallon and Cheriton. The motivation for doing so would have been help solve the problem of a shortage of 32-bit IP addresses as suggested by Asano in lines 18-30 of column 1. Therefore, it would have been obvious to combine Asano with Calvignac, Fallon and Cheriton for the benefit of helping solve the shortage of 32-bit IP addresses to obtain the invention as specified in claims 2, 5, 11, 14, 20, and 23.

8. Claims **3, 4, 12, 13, 21, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 20030231625 to Calvignac et al in view of U.S. Patent 7,415,540 to Fallon et al in view of U.S. Patent Application 2006/0104286 to Cheriton and in further view of U.S. Patent Application Publication 2004/0100956 to Watanabe.

The combination of Calvignac, Fallon and Cheriton discloses the limitations of parent claims 1, 10, and 19. However, combination of Calvignac, Fallon and Cheriton does not disclose expressly the limitations of dependent claims 3, 4, 12, 13, 21, and 22.

Regarding claims **3, 12, and 21**, Watanabe discloses the limitation that said security and classification functions comprise filtering a first data packet based on at least one of: I) a Layer 2 address associated with said first data packet; 2) a Layer 3 address associated with said first data packet; and 3) a traffic type associated with said first data packet in paragraphs 44 and 45 of page 3 which describe layer 3 addresses (IP addresses) and traffic types (service type) as areas of the header that are used by the search tree for filtering packets. Further, regarding claims **4, 13, and 22**, Watanabe discloses the limitation that said security and classification functions comprise filtering a first data packet based on at least one of: i) a Layer 4 address associated with said first data packet; and 2) a class of service (COS) value associated with said first data packet in paragraphs 52-54 of page 3 which indicates that layer 4 addresses (TCP and UDP ports) can also be used to filter the packets. Calvignac and Watanabe are analogous art because they are from the same field of endeavor of high speed packet processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to add the packet filtering means of Watanabe to the combination of Calvignac, Fallon and Cheriton. The motivation for doing so would have been to improve the security of the

network served by the router by implementing functionality such as a firewall. This is suggested by Watanabe in paragraph 4 and 10 on page 1. Therefore, it would have been obvious to combine Watanabe with the combination of Calvignac, Fallon and Cheriton for the benefit of improved security to obtain the invention as specified in claims 3, 4, 12, 13, 21, and 22.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT C. SCHEIBEL whose telephone number is 571-272-3169. The examiner can normally be reached on Mon-Fri from 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pankaj Kumar can be reached on 571-272-3011. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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